# ECE 520 ASIC Design Project Report

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1/(delay.area) (ns-1.um-2)

**8.674x10-10**

Logic Area: (um2)

**84720**

Memory: N/A

Delay (ns to run provided example).

Clock period(ns): **16.2**

# cycles: **840**

Delay (TA provided example. TA to complete)

1/(delay.area) (TA)

**ABSTRACT**

A methodology of implementing a two-layer convolution of vectors in Verilog RTL has been showcased in this project. Convolution forms the basis for Convolutional Neural Network(CNN) which are a big part of deep learning. In first layer, an array of input vectors is convoluted with filter vectors. As part of second convolution layer, the resulting vectors from the first layer are further convoluted with more filter vectors to obtain final output vectors. All vectors come and go into SRAMs, while intermediate results are registered. Hence, the first layer is a feature extraction from an input and the second layer is a fully connected layer to identify classes. Convolution is essentially multiple dot products, which essentially is being done using DesignWare Multiplier-Accumulator. Verilog was used as the HDL and synthesis of the RTL was done using Synopsys Design Compiler.

1. **INTRODUCTION**

A hardware-based approach was implemented that conducts 2-layer convolution of two 16-bit, 2’s complement vectors. Both vectors were read from different SRAMs and convoluted. Another layer of convolution was also implemented. The resulting outputs were written to yet another SRAM. The major performance metric was to minimize the area and total delay, while meeting setup and hold constraints. In Micro-Architecture section, high-level architecture drawing with interfaces will be presented and data path will be explained. In specification section, a detailed description of top-level interface and internal registers of the design will be given. In Technical Implementation section, a detailed hierarchy of the design will be presented, and controller functionality will be explained. After that verification approach, results achieved will be showcased. The flow diagram of this project is shown in Fig.1,

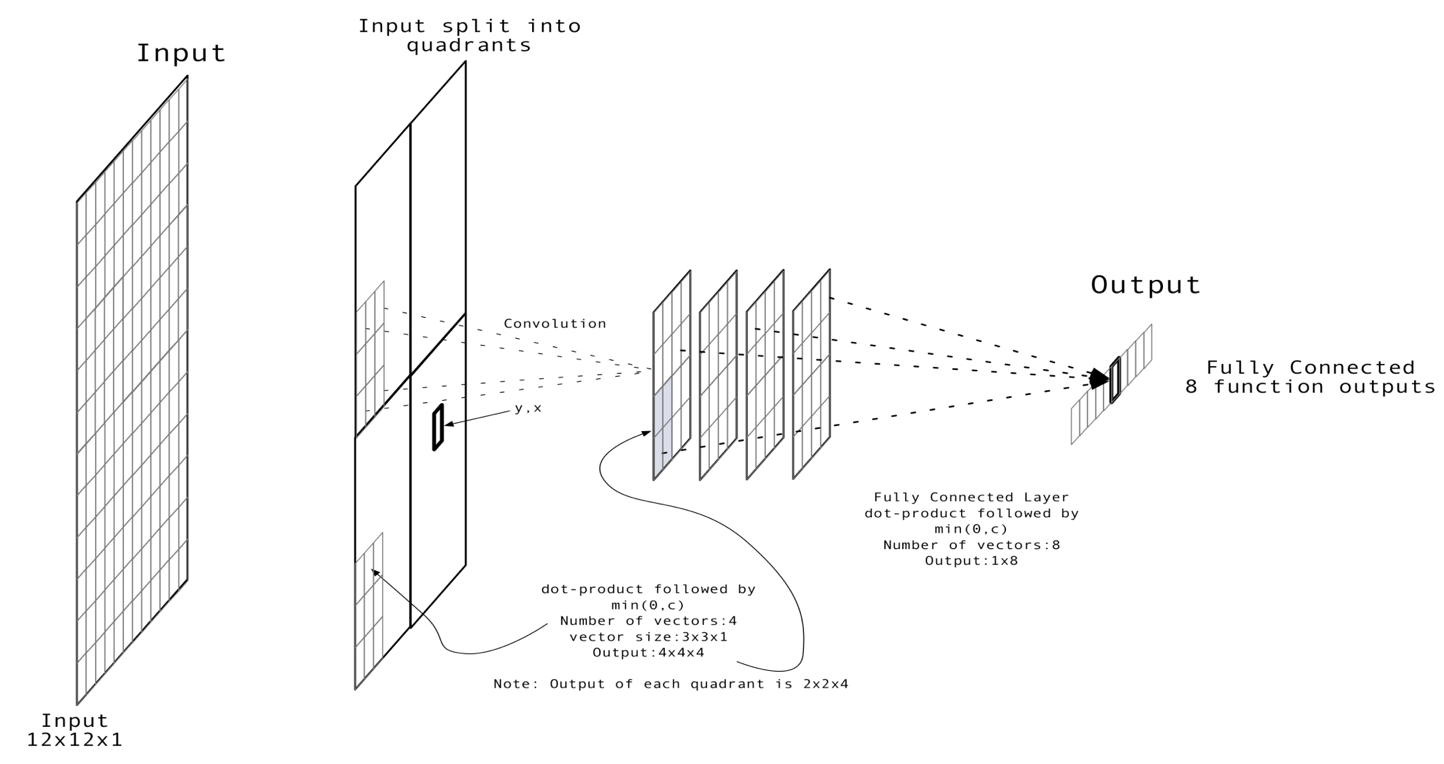


Figure 1 Project Flow Diagram

**2. MICRO-ARCHITECTURE**

Hardware “algorithmic” and “hard-coding” approach was used to do the convolution.

CNN has been well described in [1] and [2]. DesignWare Multiplier-Accumulator (DW02\_mac) was used to implement convolution.

Convolution is summation of products of two vectors, an input vector [x] and a filter vector [y] to get an output vector [z], as follows,



As stated earlier, three SRAM models were used. First SRAM contained 12x12 array of 16-bit, 2’s complement input vectors starting at address 0x0000 through 0x00BB. Second SRAM contained filter vectors, ‘b’ (for Step-1) and ‘m’ (for Step-2). The third SRAM was used to store the output memory. Fig. 2 shows detailed storage memory maps.



Figure 2 SRAM Memory Map

* **Step-1**
* The 12x12 input array was broken down into four quadrants. Each quadrant now had 6x6 input vectors. This is shown in Fig. 3,

|  |  |
| --- | --- |
| Quadrant 1  (q=1) | Quadrant 2  (q=2) |
| Quadrant 3  (q=3) | Quadrant  (q=4) |

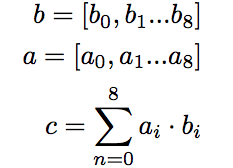
Figure 3 Input Vector Quadrants

* Each quadrant was further broken down into four parts and each part now had 3x3 input elements. Let us denote each such part as ‘i’ and ‘q’ will specify the quadrant. So, input vector can be written as a(q,i).

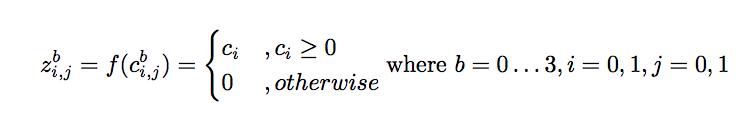
a(1,1) = {V0, V1… V8}. (Shaded)

The Fig. 4 shows detailed description of Quadrant 1.

* The 36 ‘b’ filter vectors from the second SRAM were broken down into four 1x9 sets. On each of these sets of ‘b’ dot product with a(1,1)  was performed. This gave four values of 32-bit ‘c’ as shown below,



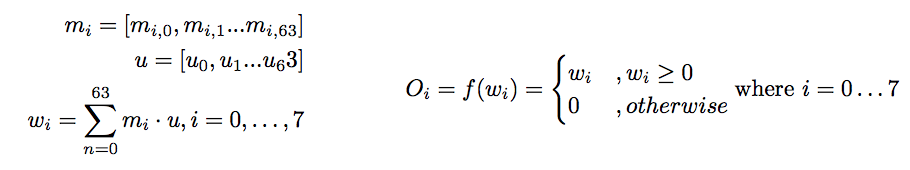
* If the same procedure is extended to all ‘a’ and ‘b’, we will get a total of sixty-four ‘c’. Then, we will perform the following operation to convert all ‘c’ into the final sixty-four outputs of Step-1, i.e., ‘z’,



|  |  |  |  |
| --- | --- | --- | --- |
| V0 | V1 | V2 | a(1,2) |
| V3 | V4 | V5 |
| V6 | V7 | V8 |
| a(1,3) | | | a(1,4) |

Figure 4 Quadrant-1 Layout

* **Step-2**
* Dot-product (convolution) was again performed in this step. Here, all ‘z’ from step-1 were separately multiplied and accumulated with each row from the 8x64 supplied ‘m’ vectors. So obtained 8 outputs were renamed as ‘w’.
* The ‘w’ were truncated and operated upon to get ‘o’ as shown below,



* **High level architecture drawing**

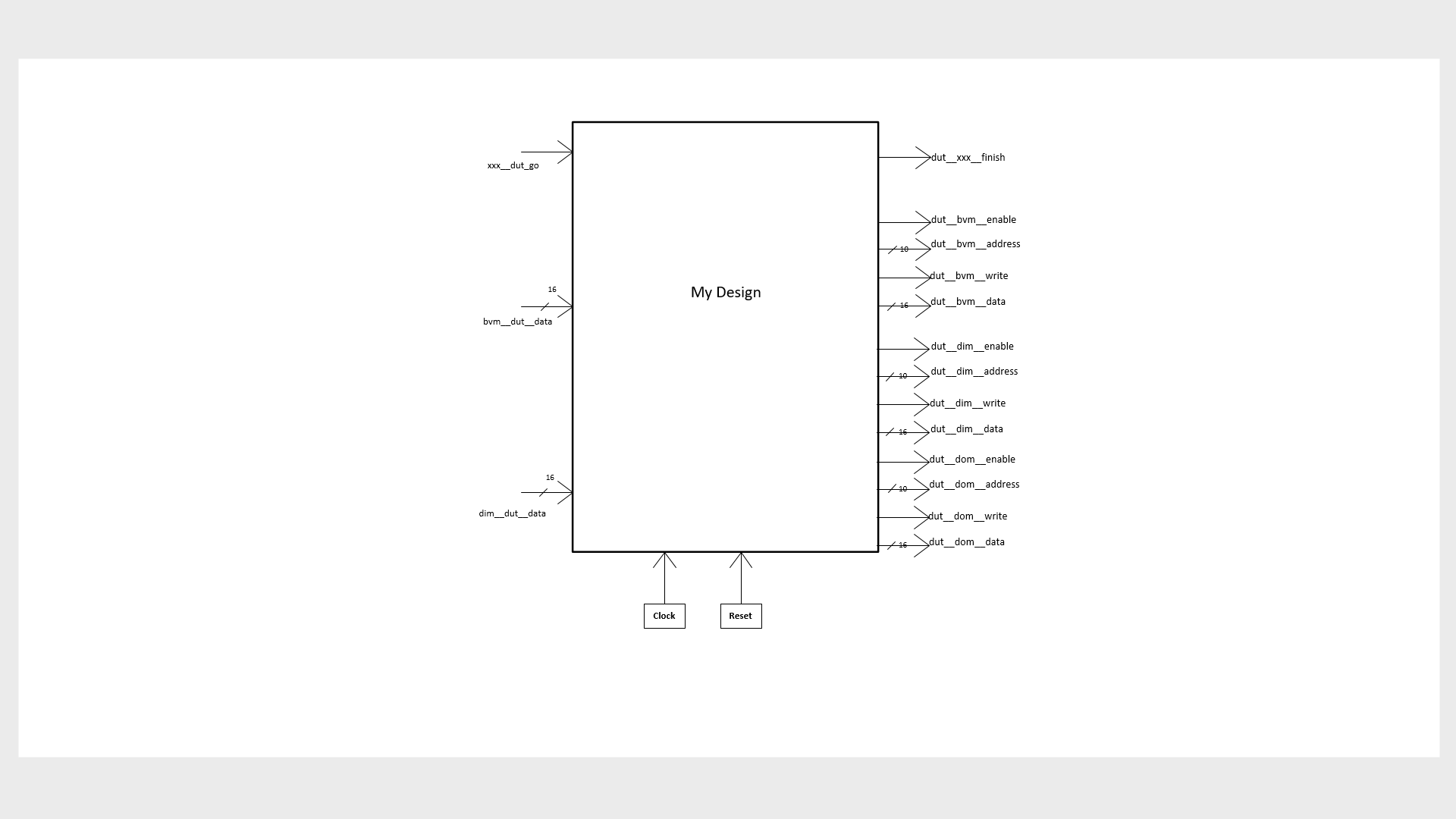


Figure 4 High Level Diagram

**3. REGISTER AND INTERFACE SPECIFICATION**

* Table listing interfacing signals, its width and function

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signals** | **Type** | **Width (bits)** | **Name** | **Comment** |
| **Control** | | | | |
| Output | reg |  | dut\_\_xxx\_finish | High when DUT is ready for a ‘go’. Deassert after ‘go |
| input | wire |  | xxx\_\_dut\_\_go | Pulsed |
| **Filter Vector Memory** | | | | |
| Output | reg | 10 | dut\_\_bvm\_\_address | To pass address to fetch data from filter vector memory |
| Output | reg |  | dut\_\_bvm\_\_enable | High for Read |
| Output | reg |  | dut\_\_bvm\_\_write | Low for Read |
| Output | reg | 16 | dut\_\_bvm\_\_data | Write Data |
| input | wire | 16 | bvm\_\_dut\_\_data | Read Data |
| **Input Data Memory** | | | | |
| Output | reg | 9 | dut\_\_dim\_\_address | To pass address to fetch data from filter vector memory |
| Output | reg |  | dut\_\_dim\_\_enable | High for Read and Write |
| Output | reg |  | dut\_\_dim\_\_write | High for Write |
| Output | reg | 16 | dut\_\_dim\_\_data | Write Data |
| input | wire | 16 | dim\_\_dut\_\_data | Read Data |
| **Output Data Memory** | | | | |
| Output | reg | 3 | dut\_\_dom\_\_address | To pass address on which the final data to be written |
| Output | reg | 16 | dut\_\_dom\_\_data | Write Data |
| Output | reg |  | dut\_\_dom\_\_enable | High for Write |
| Output | reg |  | dut\_\_dom\_\_write | High for Write |
| **General** | | | | |
| input | wire |  | clk | Clock signal |
| input | wire |  | reset | Active High |

* Table below lists registers and wires internal to the *MyDesign* module, their width and function

|  |  |  |  |
| --- | --- | --- | --- |
| **Signals** | **Type** | **Width in bits** | **Function** |
| clockCount | reg | 12 | Used to count clock cycles after ‘go’ flag is asserted |
| flag1, flag2, flag3, flag4 | reg | 1 | Used to traverse through quadrants for Step-1 |
| zReg0, zReg1,  ….zReg63 | reg | 16 | Store all output ‘z’ from Step-1 |
| mReg | reg | 16 | 16 bit register containing read data from filter SRAM |
| zTemp | reg | 16 | Used to store and input ‘z’ to MAC in Step-2 |
| oMac (‘w’ in Project specification.) | wire | 32 | Used to contain all MAC results from Step-2 |
| oTemp | reg | 32 | Used as Accumulated value in Step-2 MAC |
| oReg[7:0] | reg | 16 | Register to store final output which is then written to output SRAM |

* Table below lists registers and wires internal to the *Quadrant* module, their width and function

|  |  |  |  |
| --- | --- | --- | --- |
| **Signals** | **Type** | **Width in bits** | **Function** |
| clkCount1 | reg | 8 | Used to count clock cycles for each quadrant instantiation |
| aReg[35:0] | reg | 16 | Registers all inputs ‘a’ for a quadrant |
| bReg[35:0] | reg | 16 | Store all filter vectors ‘b’ |
| cReg | reg | 32 | Contains actual ‘c’ that is operated upon to get output of Step-1, ie, ‘z’ |
| aTemp | wire | 16 | Used to input aReg to MAC |
| bTemp[3:0] | reg | 16 | Used to input bReg to MAC |
| cTemp[3:0] | reg | 32 | Used as Accumulated value for each MAC operation |

**4. TECHNICAL IMPLEMENTATION**

Design hierarchy is as shown below I Fig. 5, Fig. 6 and Fig. 7,

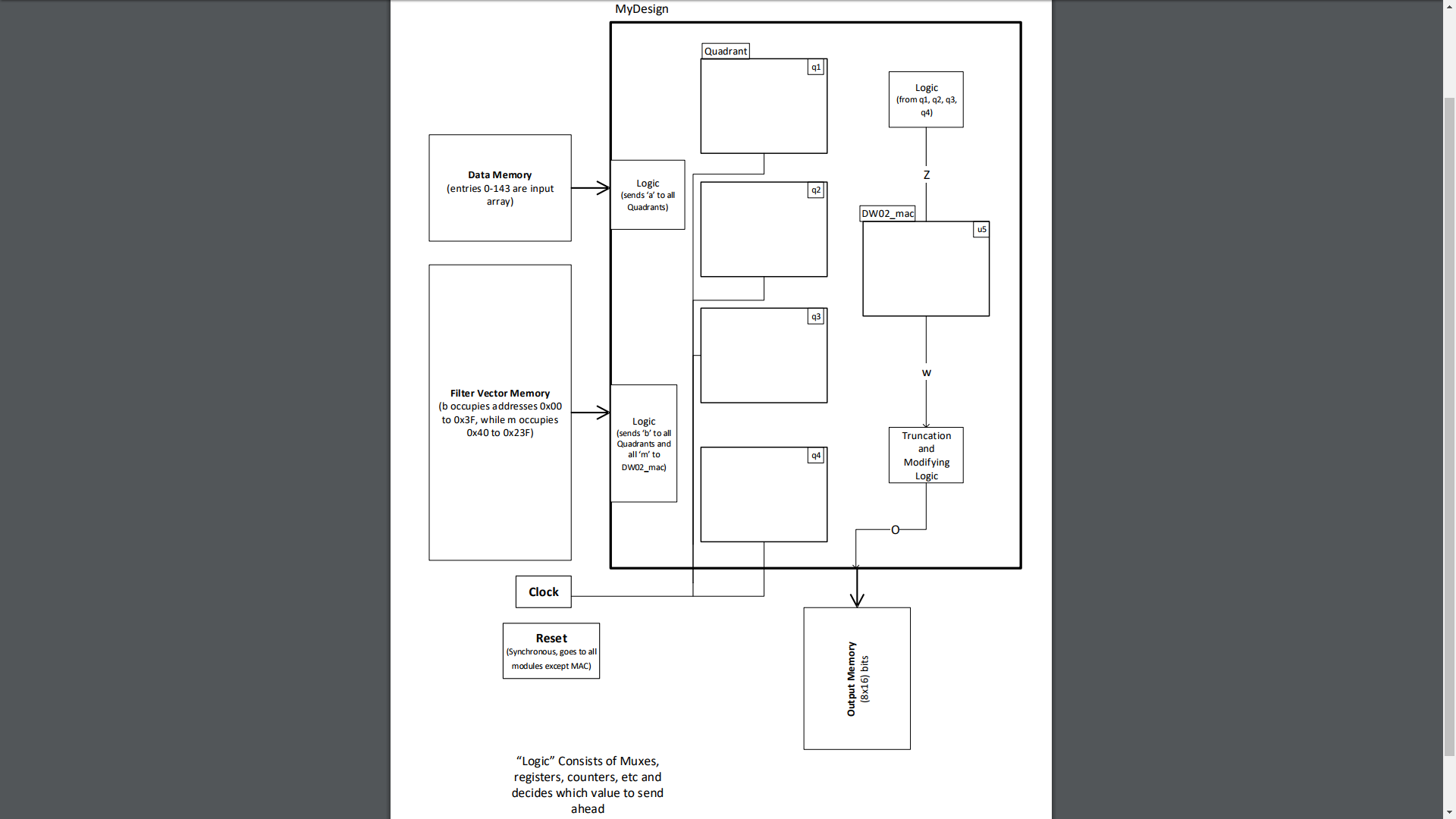


Figure 5 MyDesign Module Hierarchy

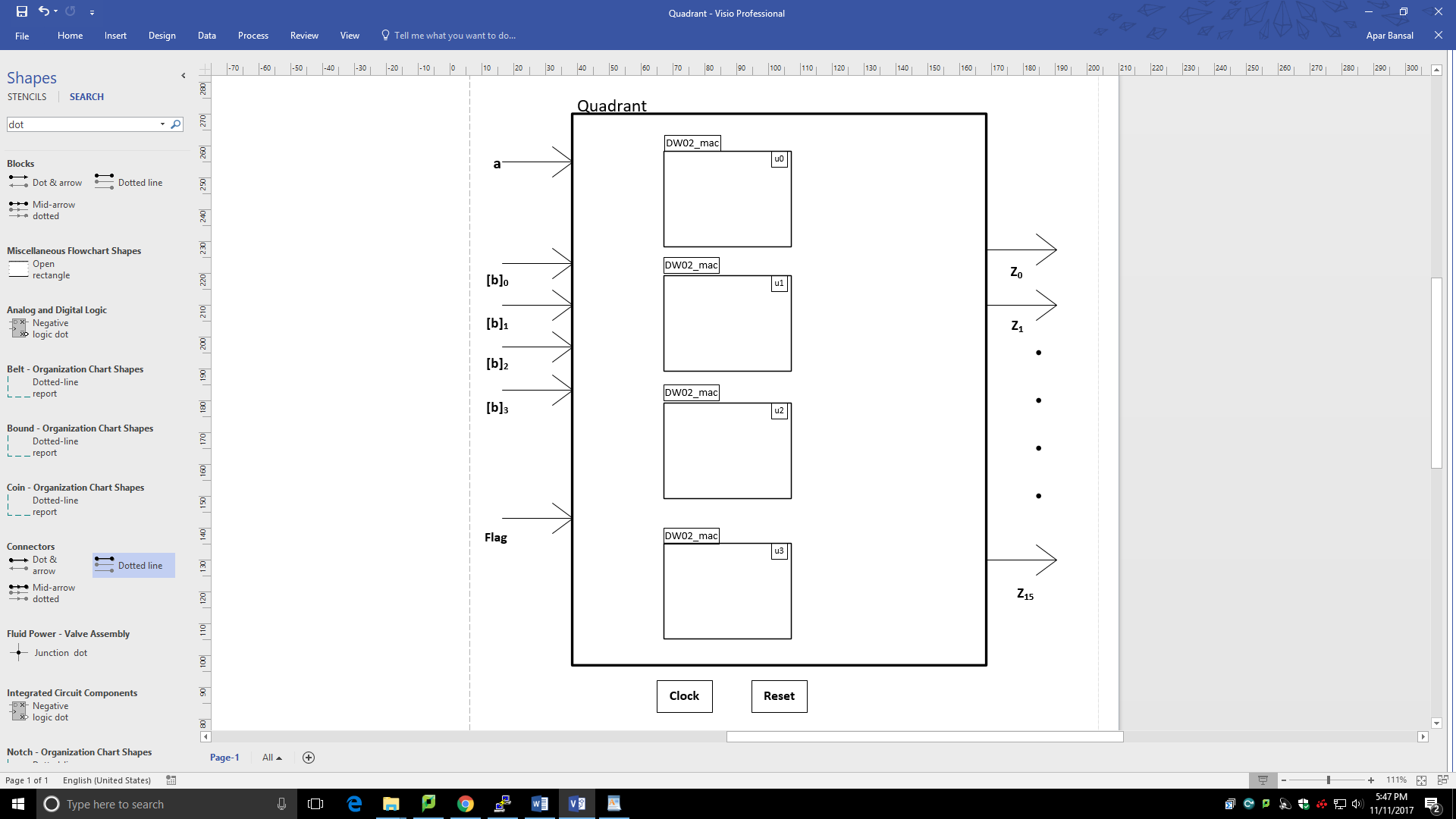


Figure 6 Quadrant Module Design

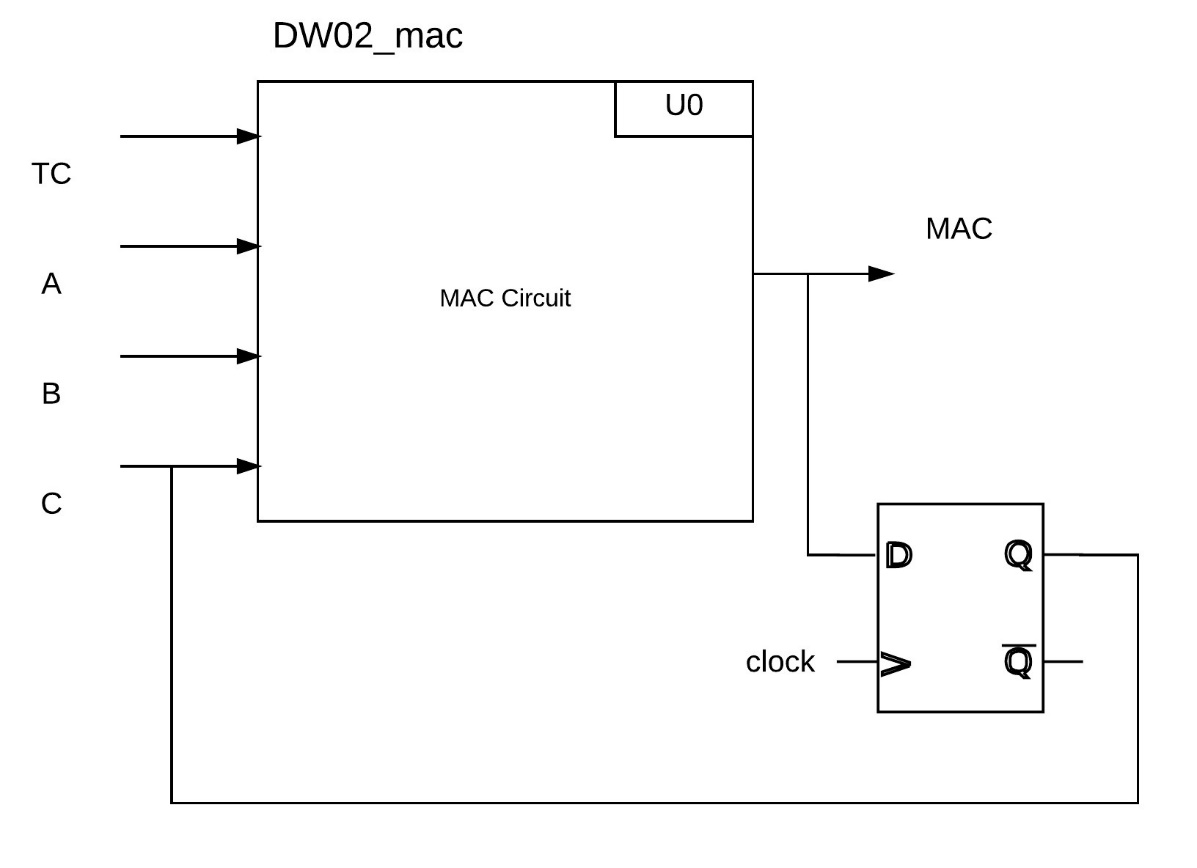


Figure 7 DW02\_mac Implementation

**Description of implementation:**

After resetting the design, a ‘go’ flag went high and a counter was then run to count clock cycles after this event. Address and data read requests were sent in to the input and filter SRAMs from the MyDesign module.

The data from the SRAMs was stored in registers in the Quadrant modules. Each quadrant was tied to a Flag that was used to activate either one of the quadrant modules at a time. The flags were controlled in the MyDesign module by the clock counter.

In each quadrant, the input (a) and filter (b) vectors were convoluted using DesignWare Multiplier-Accumulator. The resulting 32-bit (c) vectors’ first bit was checked to know its sign. If it was negative, then the output (z) was assigned as zero, else the first 16 (MSB) bits were extracted to give Step-1 output (z). This circuit is captured in Fig.8. In this way, each quadrant gave 16 ‘z’. All 4 quadrant modules outputted 64 ‘z’ in all, which were registered in 64 separate registers in MyDesign.

Then, the 8\*64, Step-2 filter (m) vectors were extracted and convoluted eight times (using a MAC in MyDesign), i.e., each row of ‘m’ was convoluted with ‘z’, thus, giving eight 32-bit outputs (w). Each of these ‘w’ were truncated and checked for sign like above, to obtain the eight final ‘o’ vectors.

Each of these ‘o’ vectors were written to an SRAM and the ‘finish’ flag was set to signal end of operation. Then, the test bench verified the simulated outputs with expected outputs.

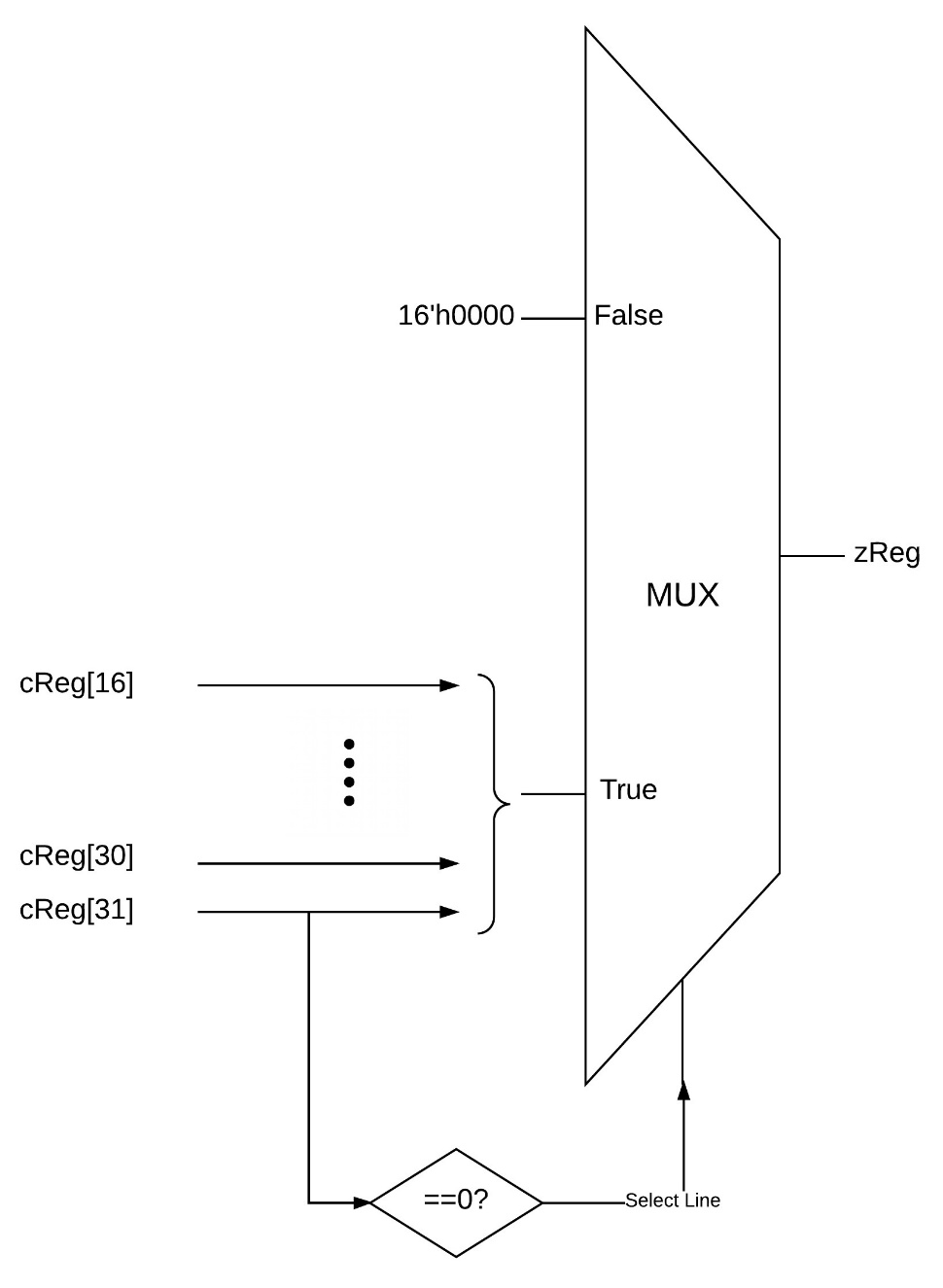


Figure 8 Truncation and Sign-Checking Circuit

**5. VERIFICATION**

A Test bench containing SRAM and logic which generate *reset*, *go* and *finish* signal is used to verify the design. Test bench reads validation input file into SRAM and generates *go* signal. And once it observes finished signal from DUT (device under test) it dumps SRAM contents to output file and ends the simulation. Output file is compared to expected result file to verify the correctness of the design. In simulation transcript, all “PASS” signify correct execution. Any error can be seen as an “ERROR” and this can be debugged by carefully observing the expected outcome and the simulation output.

**6. RESULTS ACHIEVED**

* **Timing reports**
* **Max\_slow**

Information: Updating design information... (UID-85)

Warning: Design 'MyDesign' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : MyDesign

Version: M-2016.12-SP4

Date : Sun Nov 12 13:50:55 2017

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow Library: NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10\_slow\_nldm

Wire Load Model Mode: top

Startpoint: q4/aTemp\_reg[1]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: q4/z3\_reg[0]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.0000 0.0000

clock network delay (ideal) 0.0000 0.0000

q4/aTemp\_reg[1]/CK (DFF\_X2) 0.0000 # 0.0000 r

q4/aTemp\_reg[1]/Q (DFF\_X2) 0.5836 0.5836 f

q4/U11/ZN (INV\_X4) 0.0670 0.6505 r

q4/U13/ZN (INV\_X4) 0.0622 0.7127 f

q4/U839/Z (XOR2\_X1) 0.3615 1.0742 f

q4/U545/ZN (OAI22\_X1) 0.5191 1.5933 r

q4/U1140/Z (XOR2\_X2) 0.4869 2.0802 r

q4/U1317/ZN (AOI21\_X1) 0.1527 2.2329 f

q4/U1318/ZN (AOI21\_X1) 0.6644 2.8974 r

q4/U2654/ZN (AOI21\_X2) 0.1652 3.0625 f

q4/U425/ZN (AOI21\_X2) 0.3839 3.4464 r

q4/U7908/ZN (AND2\_X4) 0.1970 3.6434 r

q4/U417/ZN (OR2\_X1) 0.1378 3.7813 r

q4/U418/ZN (NAND2\_X2) 0.1011 3.8823 f

q4/U989/ZN (OAI21\_X4) 0.1679 4.0502 r

q4/U8914/ZN (INV\_X4) 0.0474 4.0976 f

q4/U1053/ZN (AOI21\_X4) 0.3086 4.4062 r

q4/U8009/ZN (AOI21\_X2) 0.1147 4.5209 f

q4/U8850/ZN (INV\_X4) 0.0721 4.5930 r

q4/U7884/ZN (OAI21\_X2) 0.1249 4.7179 f

q4/U689/ZN (OAI21\_X4) 0.2114 4.9293 r

q4/U8813/ZN (INV\_X4) 0.0474 4.9767 f

q4/U990/ZN (AOI21\_X4) 0.3086 5.2853 r

q4/U8008/ZN (AOI21\_X2) 0.1147 5.4000 f

q4/U8722/ZN (INV\_X4) 0.0705 5.4705 r

q4/U7883/ZN (OAI21\_X2) 0.1219 5.5924 f

q4/U918/ZN (OAI21\_X4) 0.1782 5.7707 r

q4/U274/ZN (OAI21\_X2) 0.1633 5.9339 f

q4/U911/ZN (OAI21\_X4) 0.1777 6.1116 r

q4/U8622/ZN (INV\_X4) 0.0473 6.1589 f

q4/U910/ZN (AOI21\_X4) 0.3073 6.4661 r

q4/U8007/ZN (AOI21\_X2) 0.1145 6.5806 f

q4/U8578/ZN (INV\_X4) 0.0704 6.6510 r

q4/U7879/ZN (OAI21\_X2) 0.1198 6.7708 f

q4/U700/ZN (OAI21\_X4) 0.1918 6.9626 r

q4/U8546/ZN (INV\_X4) 0.0473 7.0099 f

q4/U823/ZN (AOI21\_X4) 0.2972 7.3070 r

q4/U8545/ZN (INV\_X4) 0.0694 7.3765 f

q4/U688/ZN (OAI21\_X4) 0.1503 7.5267 r

q4/U2268/ZN (OAI21\_X2) 0.1633 7.6900 f

q4/U725/ZN (OAI21\_X4) 0.1854 7.8754 r

q4/U8310/ZN (INV\_X4) 0.0473 7.9227 f

q4/U724/ZN (AOI21\_X4) 0.2972 8.2199 r

q4/U8309/ZN (INV\_X4) 0.0694 8.2893 f

q4/U646/ZN (OAI21\_X4) 0.1503 8.4395 r

q4/U7893/ZN (OAI21\_X2) 0.1666 8.6061 f

q4/U694/ZN (OAI21\_X4) 0.1865 8.7927 r

q4/U8308/ZN (INV\_X4) 0.0473 8.8400 f

q4/U626/ZN (AOI21\_X4) 0.3071 9.1471 r

q4/U8006/ZN (AOI21\_X2) 0.1144 9.2615 f

q4/U8307/ZN (INV\_X4) 0.0704 9.3319 r

q4/U7888/ZN (OAI21\_X2) 0.1232 9.4551 f

q4/U693/ZN (OAI21\_X4) 0.1876 9.6427 r

q4/U8306/ZN (INV\_X4) 0.0473 9.6900 f

q4/U537/ZN (AOI21\_X4) 0.3073 9.9973 r

q4/U8005/ZN (AOI21\_X2) 0.1145 10.1117 f

q4/U8305/ZN (INV\_X4) 0.0704 10.1821 r

q4/U2244/ZN (OAI21\_X2) 0.1168 10.2990 f

q4/U2287/ZN (INV\_X4) 0.0836 10.3826 r

q4/U2285/ZN (AOI21\_X2) 0.0643 10.4469 f

q4/U461/ZN (AOI21\_X4) 0.3295 10.7765 r

q4/U8004/ZN (AOI21\_X2) 0.1145 10.8909 f

q4/U8304/ZN (INV\_X4) 0.0678 10.9587 r

q4/U7891/ZN (OAI21\_X2) 0.1045 11.0632 f

q4/U8303/ZN (INV\_X4) 0.0957 11.1589 r

q4/U2242/ZN (AOI21\_X2) 0.0673 11.2262 f

q4/U8302/ZN (INV\_X4) 0.0704 11.2966 r

q4/U2241/ZN (OAI21\_X2) 0.1092 11.4059 f

q4/U2239/ZN (INV\_X4) 0.0834 11.4893 r

q4/U2237/ZN (AOI21\_X2) 0.0576 11.5469 f

q4/U2235/ZN (AOI21\_X2) 0.4393 11.9862 r

q4/U2625/ZN (AOI21\_X2) 0.1185 12.1047 f

q4/U256/ZN (AOI21\_X2) 0.4018 12.5065 r

q4/U8003/ZN (AOI21\_X2) 0.1289 12.6354 f

q4/U8300/ZN (INV\_X4) 0.0715 12.7070 r

q4/U2628/ZN (OAI21\_X2) 0.1038 12.8108 f

q4/U83/ZN (OAI21\_X2) 0.2327 13.0435 r

q4/U8299/ZN (INV\_X4) 0.0403 13.0838 f

q4/U2627/ZN (AOI21\_X2) 0.3592 13.4431 r

q4/U2622/ZN (AOI21\_X2) 0.1124 13.5555 f

q4/U254/ZN (AOI21\_X2) 0.4158 13.9713 r

q4/U3597/ZN (AOI21\_X2) 0.1309 14.1022 f

q4/U8220/ZN (INV\_X4) 0.0730 14.1752 r

q4/U3596/ZN (OAI21\_X2) 0.1105 14.2857 f

q4/U1313/ZN (OAI21\_X4) 0.2326 14.5183 r

q4/U3615/ZN (OAI21\_X2) 0.1344 14.6528 f

q4/U263/Z (XOR2\_X2) 0.2987 14.9515 f

q4/U260/ZN (XNOR2\_X2) 0.3495 15.3010 r

q4/U404/ZN (NAND2\_X2) 0.2151 15.5161 f

q4/U1876/ZN (OAI21\_X1) 0.3882 15.9043 r

q4/z3\_reg[0]/D (DFF\_X1) 0.0000 15.9043 r

data arrival time 15.9043

clock clk (rise edge) 16.2000 16.2000

clock network delay (ideal) 0.0000 16.2000

clock uncertainty -0.0500 16.1500

q4/z3\_reg[0]/CK (DFF\_X1) 0.0000 16.1500 r

library setup time -0.2423 15.9077

data required time 15.9077

-----------------------------------------------------------

data required time 15.9077

data arrival time -15.9043

-----------------------------------------------------------

slack (MET) 0.0034

1

* **Max\_slow\_holdfixed**

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay max

-max\_paths 1

Design : MyDesign

Version: M-2016.12-SP4

Date : Sun Nov 12 13:54:37 2017

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow Library: NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10\_slow\_nldm

Wire Load Model Mode: top

Startpoint: q4/aTemp\_reg[1]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: q4/z9\_reg[0]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: max

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.0000 0.0000

clock network delay (ideal) 0.0000 0.0000

q4/aTemp\_reg[1]/CK (DFF\_X2) 0.0000 # 0.0000 r

q4/aTemp\_reg[1]/Q (DFF\_X2) 0.5836 0.5836 f

q4/U11/ZN (INV\_X4) 0.0670 0.6505 r

q4/U13/ZN (INV\_X4) 0.0622 0.7127 f

q4/U442/ZN (NAND2\_X2) 0.1166 0.8294 r

q4/U448/ZN (NAND2\_X2) 0.0713 0.9006 f

q4/U598/ZN (INV\_X4) 0.0847 0.9853 r

q4/U29/ZN (NAND2\_X1) 0.0745 1.0598 f

q4/U33/ZN (INV\_X2) 0.1059 1.1657 r

q4/U529/ZN (INV\_X2) 0.1540 1.3197 f

q4/U3188/ZN (OAI22\_X2) 0.4565 1.7762 r

q4/U3187/Z (XOR2\_X2) 0.4407 2.2169 r

q4/U3186/ZN (XNOR2\_X2) 0.3642 2.5811 r

q4/U3185/Z (XOR2\_X2) 0.4002 2.9813 r

q4/U3184/Z (XOR2\_X2) 0.4269 3.4082 r

q4/U56/ZN (OAI22\_X2) 0.2214 3.6296 f

q4/U54/ZN (OAI21\_X4) 0.2110 3.8406 r

q4/U8896/ZN (INV\_X4) 0.0474 3.8880 f

q4/U52/ZN (AOI21\_X4) 0.3094 4.1973 r

q4/U645/ZN (OR2\_X4) 0.1980 4.3954 r

q4/U266/ZN (NAND2\_X2) 0.0724 4.4678 f

q4/U535/ZN (OAI21\_X4) 0.1634 4.6312 r

q4/U8822/ZN (INV\_X4) 0.0391 4.6703 f

q4/U106/ZN (AOI21\_X2) 0.3947 5.0650 r

q4/U7890/ZN (AOI21\_X2) 0.1312 5.1962 f

q4/U8707/ZN (INV\_X4) 0.0732 5.2695 r

q4/U7889/ZN (OAI21\_X2) 0.1190 5.3885 f

q4/U37/ZN (OAI21\_X4) 0.1964 5.5849 r

q4/U35/ZN (OAI21\_X4) 0.1393 5.7242 f

q4/U690/ZN (OAI21\_X4) 0.1678 5.8920 r

q4/U8612/ZN (INV\_X4) 0.0391 5.9311 f

q4/U104/ZN (AOI21\_X2) 0.3715 6.3027 r

q4/U7897/ZN (AOI21\_X2) 0.1289 6.4316 f

q4/U8586/ZN (INV\_X4) 0.0715 6.5031 r

q4/U7896/ZN (OAI21\_X2) 0.1201 6.6232 f

q4/U699/ZN (OAI21\_X4) 0.1937 6.8169 r

q4/U8528/ZN (INV\_X4) 0.0473 6.8642 f

q4/U2900/ZN (AOI21\_X4) 0.2972 7.1614 r

q4/U8527/ZN (INV\_X4) 0.0587 7.2200 f

q4/U265/ZN (OAI21\_X2) 0.1792 7.3992 r

q4/U2270/ZN (OAI21\_X2) 0.1730 7.5722 f

q4/U710/ZN (OAI21\_X4) 0.1854 7.7576 r

q4/U8262/ZN (INV\_X4) 0.0473 7.8050 f

q4/U2801/ZN (AOI21\_X4) 0.2972 8.1021 r

q4/U8261/ZN (INV\_X4) 0.0587 8.1608 f

q4/U246/ZN (OAI21\_X2) 0.1792 8.3400 r

q4/U2045/ZN (OAI21\_X2) 0.1652 8.5052 f

q4/U713/ZN (OAI21\_X4) 0.1829 8.6881 r

q4/U8260/ZN (INV\_X4) 0.0391 8.7272 f

q4/U95/ZN (AOI21\_X2) 0.3713 9.0985 r

q4/U2273/ZN (AOI21\_X2) 0.1289 9.2274 f

q4/U8259/ZN (INV\_X4) 0.0715 9.2989 r

q4/U2272/ZN (OAI21\_X2) 0.1038 9.4027 f

q4/U244/ZN (OAI21\_X2) 0.2327 9.6354 r

q4/U8258/ZN (INV\_X4) 0.0403 9.6757 f

q4/U2233/ZN (AOI21\_X2) 0.3950 10.0707 r

q4/U2279/ZN (AOI21\_X2) 0.1309 10.2016 f

q4/U8257/ZN (INV\_X4) 0.0730 10.2746 r

q4/U2277/ZN (OAI21\_X2) 0.1135 10.3881 f

q4/U8256/ZN (INV\_X4) 0.0859 10.4740 r

q4/U2231/ZN (AOI21\_X2) 0.0582 10.5322 f

q4/U2229/ZN (AOI21\_X2) 0.4137 10.9459 r

q4/U2304/ZN (AOI21\_X2) 0.1309 11.0767 f

q4/U8255/ZN (INV\_X4) 0.0730 11.1498 r

q4/U2303/ZN (OAI21\_X2) 0.1023 11.2520 f

q4/U2250/ZN (INV\_X4) 0.0984 11.3504 r

q4/U2248/ZN (AOI21\_X2) 0.0679 11.4183 f

q4/U8254/ZN (INV\_X4) 0.0704 11.4887 r

q4/U2246/ZN (OAI21\_X2) 0.1092 11.5980 f

q4/U2295/ZN (INV\_X4) 0.0817 11.6796 r

q4/U2293/ZN (AOI21\_X2) 0.0571 11.7368 f

q4/U242/ZN (AOI21\_X2) 0.3908 12.1275 r

q4/U7965/ZN (AOI21\_X2) 0.1142 12.2417 f

q4/U93/ZN (AOI21\_X2) 0.3971 12.6388 r

q4/U8042/ZN (AOI21\_X2) 0.1289 12.7677 f

q4/U8253/ZN (INV\_X4) 0.0715 12.8392 r

q4/U7904/ZN (OAI21\_X2) 0.1038 12.9431 f

q4/U77/ZN (OAI21\_X2) 0.2327 13.1758 r

q4/U8252/ZN (INV\_X4) 0.0403 13.2161 f

q4/U75/ZN (AOI21\_X2) 0.3310 13.5471 r

q4/U7963/ZN (AOI21\_X2) 0.1204 13.6675 f

q4/U17/ZN (AOI21\_X4) 0.3396 14.0071 r

q4/U7895/ZN (AOI21\_X2) 0.1167 14.1238 f

q4/U8206/ZN (INV\_X4) 0.0678 14.1916 r

q4/U7894/ZN (OAI21\_X2) 0.1009 14.2925 f

q4/U230/ZN (OAI21\_X2) 0.2474 14.5399 r

q4/U3610/ZN (OAI21\_X2) 0.1431 14.6830 f

q4/U2340/Z (XOR2\_X2) 0.2999 14.9829 f

q4/U2337/ZN (XNOR2\_X2) 0.2828 15.2657 f

q4/U135/ZN (NAND2\_X2) 0.1325 15.3982 r

q4/U7909/Z (BUF\_X4) 0.2819 15.6801 r

q4/U8034/ZN (OAI21\_X2) 0.1304 15.8105 f

q4/z9\_reg[0]/D (DFF\_X2) 0.0000 15.8105 f

data arrival time 15.8105

clock clk (rise edge) 16.2000 16.2000

clock network delay (ideal) 0.0000 16.2000

clock uncertainty -0.0500 16.1500

q4/z9\_reg[0]/CK (DFF\_X2) 0.0000 16.1500 r

library setup time -0.3322 15.8178

data required time 15.8178

-----------------------------------------------------------

data required time 15.8178

data arrival time -15.8105

-----------------------------------------------------------

slack (MET) 0.0073

1

* Min\_fast\_holdcheck

Information: Updating design information... (UID-85)

Warning: Design 'MyDesign' contains 1 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : timing

-path full

-delay min

-max\_paths 1

Design : MyDesign

Version: M-2016.12-SP4

Date : Sun Nov 12 13:52:02 2017

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

# A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: fast Library: NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10\_fast\_nldm

Wire Load Model Mode: top

Startpoint: oTemp\_reg[31]

(rising edge-triggered flip-flop clocked by clk)

Endpoint: oTemp\_reg[31]

(rising edge-triggered flip-flop clocked by clk)

Path Group: clk

Path Type: min

Point Incr Path

-----------------------------------------------------------

clock clk (rise edge) 0.0000 0.0000

clock network delay (ideal) 0.0000 0.0000

oTemp\_reg[31]/CK (DFF\_X2) 0.0000 # 0.0000 r

oTemp\_reg[31]/QN (DFF\_X2) 0.0501 0.0501 f

U255/ZN (OAI22\_X2) 0.0224 0.0724 r

oTemp\_reg[31]/D (DFF\_X2) 0.0000 0.0724 r

data arrival time 0.0724

clock clk (rise edge) 0.0000 0.0000

clock network delay (ideal) 0.0000 0.0000

clock uncertainty 0.0500 0.0500

oTemp\_reg[31]/CK (DFF\_X2) 0.0000 0.0500 r

library hold time -0.0165 0.0335

data required time 0.0335

-----------------------------------------------------------

data required time 0.0335

data arrival time -0.0724

-----------------------------------------------------------

slack (MET) 0.0389

1

* Area report

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Report : area

Design : MyDesign

Version: M-2016.12-SP4

Date : Sun Nov 12 13:59:43 2017

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Library(s) Used:

NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10\_slow\_nldm (File: /afs/eos.ncsu.edu/lockers/research/ece/wdavis/tech/nangate/NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10/liberty/520/NangateOpenCellLibrary\_PDKv1\_2\_v2008\_10\_slow\_nldm.db)

Number of ports: 2488

Number of nets: 50528

Number of cells: 43980

Number of combinational cells: 37222

Number of sequential cells: 6742

Number of macros/black boxes: 0

Number of buf/inv: 4909

Number of references: 56

Combinational area: 52468.766581

Buf/Inv area: 2625.952025

Noncombinational area: 32251.968719

Macro/Black Box area: 0.000000

Net Interconnect area: undefined (No wire load specified)

Total cell area: 84720.735301

Total area: undefined

1

* Simulation snapshots

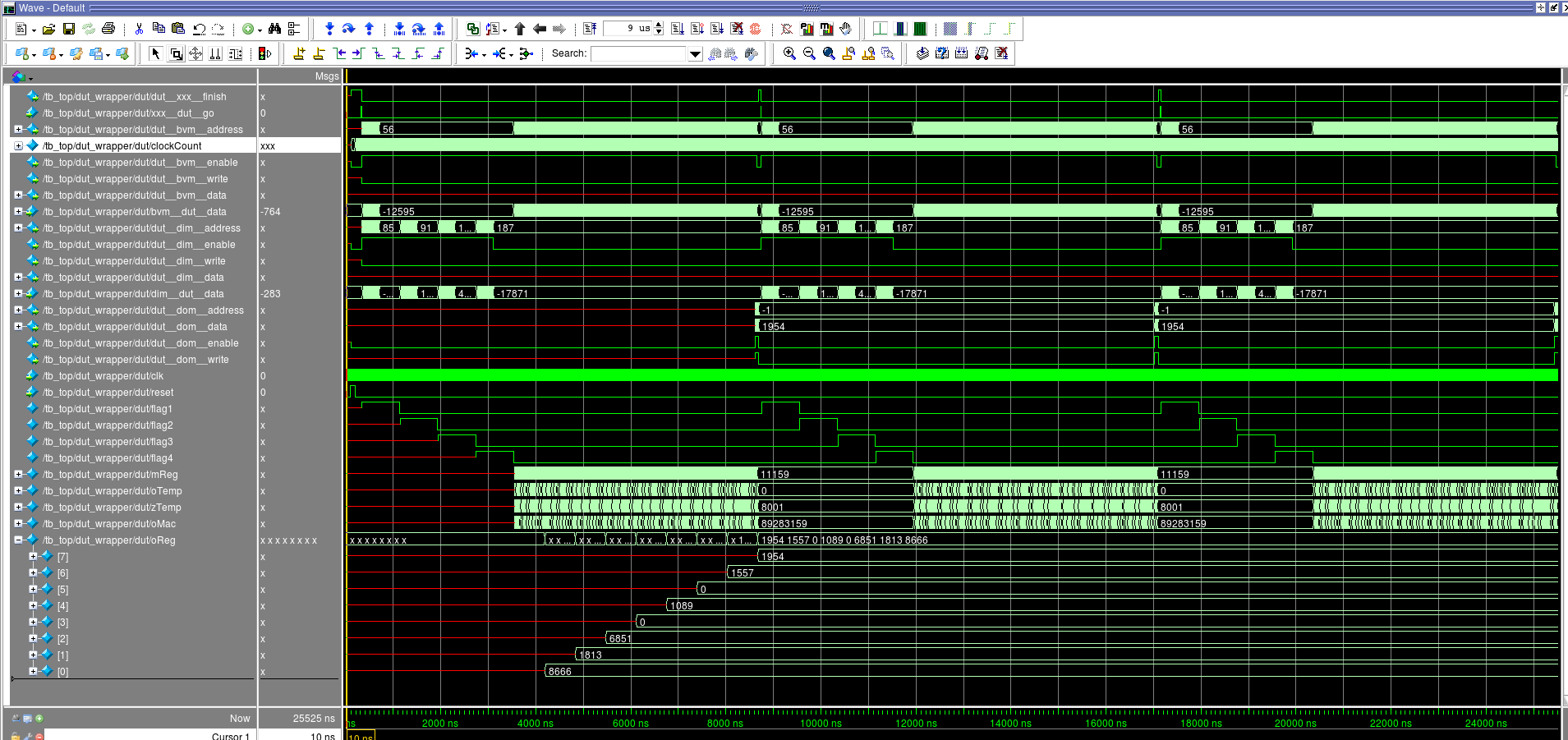


Figure 9 Simulation Wave for MyDesign Module

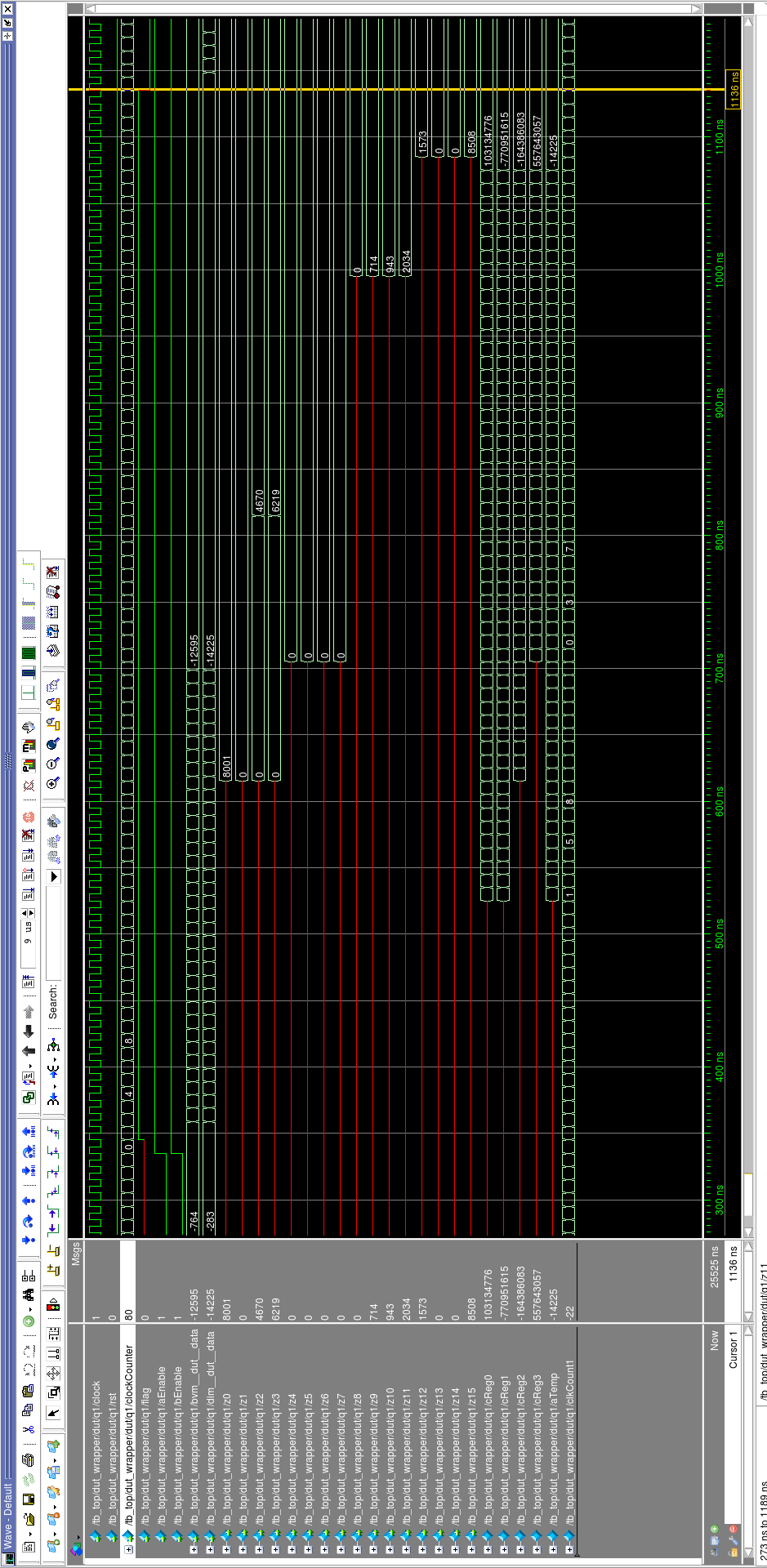


Figure 10 Simulation Wave for First Quadrant, u0

**7. CONCLUSIONS**

A 2-layer convolution hardware has been successfully designed with Verilog and synthesized using Synopsys Design Compiler. Below is the summary of the results obtained.

Clock period = 16.2 ns

Execution time = 840 cycles

Area obtained = 84720 um2

Total Power = 2.2795 mW

**REFERENCES**

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[2]. Saxena, Abhineet, “Convolutional Neural Networks(CNNs): An Illustrated Explanantion”. XRDS Crossroads. http://xrds.acm.org/blog/2016/06/convolutional-neural-networks-cnns-illustrated-explanation/

[3]. Sutherland, Stuart. “Verilog HDL Quick Reference Guide, based on the Verilog-2001 Standard”, 2001. Sutherland HDL, Inc.

[4]. Smith and Franzon, Paul, “Verilog Styles for Synthesis of Digital Systems”, 2000, Prentice Hall.

[5]. NCSU ASIC Design Tutorials. (Retrieved on Nov 10, 2017) <https://www.eda.ncsu.edu/wiki/Tutorial:ASIC_Design_Tutorials>